WHAT IS CLAIMED IS:

1. An organic electroluminescent display (ELD) device, comprising:

first and second substrates having a plurality of sub-pixels defined thereon;

an array element layer on the first substrate having a plurality of thin film transistors corresponding to each of the sub-pixels;

a connecting electrode on the array element layer connected to one of the thin film transistors;

a first electrode on an inner surface of the second substrate;

an insulating layer and an electrode separator formed within a boundary region of each of the sub-pixels, the insulating layer formed beneath the first electrode and the electrode separator formed beneath the insulating layer; and

an organic light-emitting layer and a second electrode formed in each of the sub-pixels,

wherein the electrode separator includes a first region having a pattern structure for separately forming the organic light-emitting layer and the second electrode within each of the sub-pixels, a second region having a pattern structure for directly contacting the connecting electrode with the second electrode under the electrode separator, and a third region having a pattern structure for preventing an

electrical short between a second electrode portion in the first region and a second electrode portion in the second region, and

wherein the second electrode formed within a space corresponding to the second region contacts the connecting electrode.

2. The device according to claim 1, wherein the electrode separator of the first region has a trapezoidal shape having a width gradually increasing from a bottom surface and to a top surface, the electrode separator of the second region has an asymmetrical shape having an inverse-tapered first lateral side and a second lateral side inclined toward the first lateral side, and the electrode separator of the third region has a plurality of depressed portions.

3. The device according to claim 2, wherein the electrode separators of the second and third regions are formed by a diffraction exposure method.

4. The device according to claim 1, wherein the first and second electrodes and the organic light-emitting layer form an organic electroluminescent diode, and the thin film transistor has a gate electrode, a semiconductor layer, and source and drain electrodes, wherein the thin film transistor is a driving thin film transistor for

supplying a current to the organic electroluminescent diode and the connecting electrode is electrically connected to the drain electrode.

5. The device according to claim 4, further comprising a projected region having a laminated structure on the first substrate, wherein a height of the laminated structure is larger than a height of the array element layer, and the connecting electrode contacts the second electrode over the projected region.

6. The device according to claim 5, wherein first, second, and third patterns have island shaped patterns and are simultaneously formed within the projected region during formation of the gate electrode, the semiconductor layer, and the source and drain electrodes, respectively, using the same materials as the gate electrode, the semiconductor layer, and the source and drain electrodes.

7. The device according to claim 6, further comprising a power supply line connected to the source electrode, and a fourth pattern over the third pattern, wherein the fourth pattern and the power supply line are simultaneously formed using the same materials.

8. The device according to claim 1, further comprising a passivation layer having a drain contact hole exposing a portion of the drain electrode, a projected pattern on the passivation layer within the projected region, and a connecting electrode on the projected pattern, wherein the connecting electrode contacts the drain electrode via the drain contact hole.

9. The device according to claim 8, wherein the projected pattern is formed of insulating material.

10. The device according to claim 9, wherein the insulating material includes organic insulating material.

11. A method of fabricating an organic electroluminescent display (ELD) device having a first substrate including an array element layer comprising a thin film transistor, a second substrate having an organic electroluminescent diode, and a connecting electrode between the first and second substrates, the method comprising:

forming a first electrode on the second substrate having a plurality of sub-pixels;

forming an insulating layer and an electrode separator within a boundary of each of the sub-pixels; and

forming an organic light-emitting layer and a second electrode within each of the sub-pixels separated by the electrode separator,

wherein the electrode separator includes a first region having a trapezoidal shape with a width gradually increasing from a bottom surface and to a top surface, a second region having an asymmetrical shape with a first inverse-tapered lateral side and a second lateral side inclined toward the first lateral side, and a third region having a plurality of depressed portions spaced apart from each other and disposed between the first and second regions, and

wherein the second electrode is formed within a space corresponding to the second region and contacts the connecting electrode.

12. The method according claim 11, further comprising attaching the first and second substrates together after forming the organic light-emitting layer and the second electrode, wherein the first and second substrates are electrically interconnected by contacting the connecting electrode with the second electrode.

13. The method according claim 11, wherein the electrode separator is formed by a diffraction exposure method.

14. The method according claim 13, wherein the electrode separator of the second region is formed by controlling widths of light transmission portions and intervals between the light transmission portions of a mask for the diffraction exposure method.

15. The method according claim 13, wherein the electrode separator of the third region is formed by the diffraction exposure method using a mask having a slit pattern corresponding to the depressed portion.

16. The method according claim 11, wherein the thin film transistor includes a gate electrode, a semiconductor layer, a source electrode, a drain electrode, and a power supply line.

17. The method according claim 16, wherein the array element layer further comprises a projected region having a laminated structure having a height larger than a height of the thin film transistor, and the connecting electrode contacts the second electrode over the projected region.

18. The method according claim 17, further comprising attaching the first and second substrates together after forming the organic light-emitting layer and the second electrode, wherein the first and second substrates are electrically interconnected by contacting the connecting electrode with the second electrode over the projected region.

19. The method according claim 17, wherein the laminated structure of the projected region has first, second, third, and fourth patterns overlapping each other that are formed simultaneously with the gate electrode, the semiconductor layer, the source and drain electrodes, and the power supply line using the same materials as the gate electrode, the semiconductor layer, the source and drain electrodes, and the power supply line, respectively.

20. The method according claim 17, further comprising forming a passivation layer having a drain contact hole for exposing a portion of the drain electrode on the thin film transistor, and forming a projected pattern on the passivation layer within a space corresponding to the projected region.

21. The method according claim 20, wherein the projected pattern includes organic insulating material.

22. A method for fabricating an organic electroluminescent display (ELD) device, comprising:

forming an array element layer having a plurality of thin film transistors on a first substrate upon which a first plurality of sub-pixels is defined;

forming a connecting electrode connected to the thin film transistor on the array element layer;

forming a first electrode on a second substrate upon which a second plurality of sub-pixels is defined that correspond to the first plurality of sub-pixels;

forming an insulating layer and an electrode separator within a boundary of each of the first and second plurality of sub-pixels;

forming an organic light-emitting layer and a second electrode within each of the first and second plurality of sub-pixels separated by the electrode separator; and

attaching the first and second substrates together,

wherein the electrode separator has a first region having a trapezoidal shape with a width gradually increasing from a bottom surface and to a top surface, a second region having an asymmetrical shape with a first inverse-tapered lateral side and a second lateral side inclined toward the first lateral side, and a third region having a plurality of depressed portions spaced apart from each other and disposed between the first and second regions, and

wherein the second electrode is formed within a space corresponding to the second region and contacts the connecting electrode.

23. The method according claim 22, wherein the electrode separator is formed by a diffraction exposure method.

24. The method according claim 23, wherein the electrode separator of the second region is formed by controlling widths of light transmission portions and intervals between the light transmission portions of a mask for the diffraction exposure method.

25. The method according claim 23, wherein the electrode separator of the third region is formed by the diffraction exposure method using a mask having a slit pattern corresponding to the depressed portion.

26. The method according claim 22, wherein the thin film transistor includes a gate electrode, a semiconductor layer, a source electrode, a drain electrode, and a power supply line.

27. The method according claim 26, wherein the array element layer further comprises a projected region having a laminated structure having a height larger than a height of the thin film transistor, and the connecting electrode contacts the second electrode over the projected region.

28. The method according claim 27, wherein the laminated structure of the projected region includes first, second, third, and fourth patterns overlapping each other that are formed simultaneously with the gate electrode, the semiconductor layer, the source and drain electrodes, and the power supply line using the same materials as the gate electrode, the semiconductor layer, the source and drain electrodes, and the power supply line, respectively.

29. The method according claim 27, further comprising forming a passivation layer having a drain contact hole exposing a portion of the drain electrode on the thin film transistor, and forming a projected pattern on the passivation layer within a space corresponding to the projected region.

30. The method according claim 30, wherein the projected pattern includes organic insulating material.